

---

# Full-Duplex LVDS Interface (v3.00.a)

---

## Introduction

The Full-Duplex LVDS interface described in this document provides designers with a flexible, easy-to-use method of connecting two FPGAs using a high-speed parallel LVDS bus. The design provides circuitry for clock forwarding, detection and recovery, serialization and de-serialization of parallel data, automatic training and alignment of data busses, clock domain crossing, as well as automatic link renegotiation if a link partner is reset, reprogrammed or hot-swapped. Users are presented with an abstracted synchronous FIFO interface of configurable width to exchange data with link partners.

## Features

- Compatible with Xilinx Virtex-5™ and Virtex-6™ FPGA families
- Compatible with Xilinx ISE™/EDK™ versions 10.1.03 and later
- Dedicated OSERDES/ISERDES/IDDR/ODDR and BUFIO/BUFR resources used to serialize and de-serialize LVDS data, minimizing slice resource utilization and improving timing closure
- Clock-forwarded interface eliminates need to minimize clock skew between link partners
- Clock-detection circuitry automatically detects loss of link partner and re-negotiates link once partner returns on-line
- Intelligent training procedure automatically detects and corrects for bit slips in serialization-deserialization, and accounts for any LVDS polarity flips between link partners
- Asynchronous FIFOs incorporated within design to transfer data between recovered clock domain and user-logic clock domain
- User-specified serialization/deserialization ratios between 1:1 and 6:1
- Core provides status output to hold user logic in reset until link is negotiated
- Multiple I/O banks can be aggregated to provide wide datapaths
- Dedicated circuitry available for LVDS data recovery using non-standard configurations (center-column banks used as inputs in Virtex-5, receiving clock not connected to clock-capable inputs, etc.)

## Functional Description

The top-level block diagram for the LVDS transceiver core is shown in Figure 1. The transmit and receive units operate independently of each other, however, the control information is tightly coupled between these units.

### Clocking Requirements

The user must provide four clock signals generated from the same PLL:

- 1) A user clock signal. It is expected that this signal operates at the same clock frequency as the rest of the FPGA core logic, however, asynchronous FIFOs can be used to interface to logic operating at different clock frequencies.
- 2) A transmit clock signal. The frequency of this signal is determined by the specified serialization ratio. For example, specifying a 4:1 DDR serialization ratio requires that the transmit clock frequency is exactly twice that of the user clock frequency.
- 3) A phase-delayed copy of the transmit clock signal. This signal can be generated by specifying the static phase offset of the PLL output to 90°.
- 4) A 200MHz reference clock signal to calibrate the IODELAY controller elements (not shown in Figure 1).

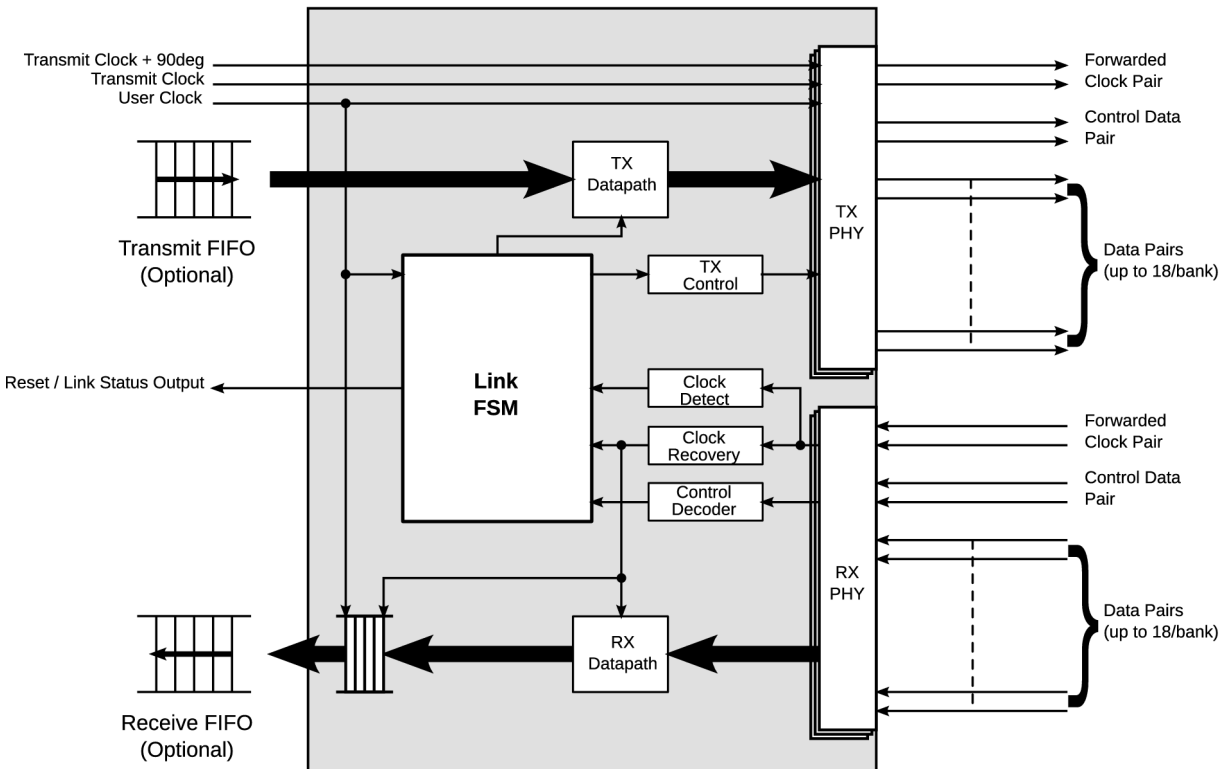


Figure 1: LVDS Transceiver Core Top Level Diagram

## I/O Resource Requirements

The LVDS interface is designed such that each PHY must be contained within a single I/O bank. Each PHY requires a minimum of two LVDS pairs: one for forwarding a clock signal, and up to three for control information (depending on the serialization factor, as seen in Table 1). The remaining LVDS pairs within the banks can be used for the datapath. Several PHYs can be aggregated across multiple banks to increase the data width of the LVDS interface, however, each bank must reserve LVDS pairs for clock forwarding and control information.

It is assumed that the LVDS signals are connected to the FPGA in a manner that is consistent with the capabilities of the FPGA:

- The forwarded clock signal is connected to a CCLK-capable input of the RX PHY.
- The data skew between individual LVDS pairs within a bank is minimized (< 30ps).
- In Virtex-5 devices, the receive bank cannot be located in the center column of the device due to lack of BUFR resources.

Work-arounds are possible for each restriction in some cases. Contact ArchES Computing for more information.

**Table 1: Control Signal LVDS Signal Requirements (per Bank)**

Serialization Factor	Number of LVDS Clock Pairs	Number of LVDS Control Pairs	Bits Available for Datapath
1:1	1	3	0
2:1	1	2	1
3:1	1	1	0
4:1	1	1	1
5:1	1	1	2
6:1	1	1	3

## Interface Performance

Table 2 illustrates the LVDS interface performance under a variety of supported configurations. The table is organized into three sections: the first section illustrates the effect of the serialization ratio on the required transmit clock frequency and the maximum user interface width. The second section of Table 2 shows how the user interface width grows as multiple banks are used for the RX and TX PHYs. The final section compares the overhead of the LVDS interface core under various serialization settings when only one LVDS pair is used to transmit data and the remainder are used for clock forwarding and control data.

Table 2: LVDS Transceiver Interface Performance

User Clock (MHz)	Transmit Clock <sup>(1)</sup> (MHz)	No. RX Banks	No. TX Banks	LVDS pairs / bank	Serialization Ratio	Maximum User Interface Width <sup>(2)</sup>	Data Rate / LVDS pair <sup>(3)</sup>	Total Data Rate
<i>User Clock = 100MHz, 1 RX Bank, 1 TX Bank, 20 LVDS pairs/bank.</i>								
100MHz	100MHz	1	1	20	1:1 (SDR)	16 bits	100 Mbps	1.60 Gbps
100MHz	200MHz	1	1	20	2:1 (SDR)	35 bits	200 Mbps	3.50 Gbps
100MHz	100MHz	1	1	20	2:1 (DDR)	35 bits	200 Mbps	3.50 Gbps
100MHz	300MHz	1	1	20	3:1 (SDR)	54 bits	300 Mbps	5.40 Gbps
100MHz	400MHz	1	1	20	4:1 (SDR)	73 bits	400 Mbps	7.30 Gbps
100MHz	200MHz	1	1	20	4:1 (DDR)	73 bits	400 Mbps	7.30 Gbps
100MHz	500MHz	1	1	20	5:1 (SDR)	92 bits	500 Mbps	9.20 Gbps
100MHz	600MHz	1	1	20	6:1 (SDR)	111 bits	600 Mbps	11.1 Gbps
100MHz	300MHz	1	1	20	6:1 (DDR)	111 bits	600 Mbps	11.1 Gbps
<i>User Clock = 200MHz, 20 LVDS pairs/bank, 4:1 DDR Serialization.</i>								
200MHz	400MHz	0.5 <sup>(4)</sup>	0.5 <sup>(4)</sup>	10	4:1 (DDR)	33 bits	800 Mbps	6.60 Gbps
200MHz	400MHz	1	1	20	4:1 (DDR)	73 bits	800 Mbps	14.6 Gbps
200MHz	400MHz	2	2	20	4:1 (DDR)	146 bits	800 Mbps	29.2 Gbps
200MHz	400MHz	4	4	20	4:1 (DDR)	292 bits	800 Mbps	58.4 Gbps
<i>User Clock = 100MHz, 1 RX Bank, 1 TX Bank, Single LVDS pair for data.</i>								
100MHz	100MHz	1	1	5	1:1 (SDR)	1 bit	100 Mbps	0.10 Gbps
100MHz	100MHz	1	1	4	2:1 (DDR)	3 bits	200 Mbps	0.30 Gbps
100MHz	300MHz	1	1	3	3:1 (SDR)	3 bits	300 Mbps	0.30 Gbps
100MHz	200MHz	1	1	3	4:1 (DDR)	5 bits	400 Mbps	0.50 Gbps
100MHz	500MHz	1	1	3	5:1 (SDR)	7 bits	500 Mbps	0.70 Gbps
100MHz	300MHz	1	1	3	6:1 (DDR)	9 bits	600 Mbps	0.90 Gbps
<p>(1) Transmit Clock frequency may be restricted by device I/O or clock buffer switching characteristics. DDR serialization modes are recommended to reduce operating frequency requirements. Consult device datasheet for maximum allowable clock frequencies.</p> <p>(2) Maximum User Interface Width includes additional data bits provided by control signals. Refer to Table 1 for number of additional data bits available.</p> <p>(3) Data rate per LVDS pair may be limited by LVDS bus skew and signal integrity. All tests for 800Mbps conducted using LVDS banks with &lt; 10ps of data skew per bank.</p> <p>(4) Receive and Transmit PHYs are packed into same I/O bank in this configuration.</p>								